30.9 A 240MHz-BW 112dB-DR TIA

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Some of the most crucial requirements on the optical receiver are its bandwidth (BW) and dynamic range (DR). DR is defined here as the ratio of maximum-to-minimum input photocurrent that can still be sensed by the optical receiver. The lower bound of the DR is the noise produced by the front end of the receiver. While the upper bound of DR is the maximum input current that can still be handled properly. Common optical receivers have DR mainly determined by the feedback resistor of the TIA. This feedback resistor also affects the BW of the TIA and thus directly controls the trade-off between DR and BW.

In the conventional optical-receiver design a sufficient DR can be achieved by switching several feedback resistors [1], by placing an automatic gain control [2] or a limiting-amplifier stage after the preamplifier. However, these techniques do not prevent the preamplifier from saturating at high input currents. A saturated TIA does not respond to the input current and it recovers very slowly back to the normal-operation mode. Therefore, the saturation of TIA, caused by high input currents, strongly degrades the pulse response of the complete optical receiver.

A wide-DR TIA with monotonic compression of input current up to 8mA and with maximal current-overdrive capability up to 20mA is presented. The measured BW is 240MHz. The equivalent rms input-current noise is 48nA within the BW and with 2pF photodiode capacitance at the input. The proposed design is intended for use in optical sensing applications, but it is also suited for other applications such as LAN technologies, optical data-storage systems, wireless IR links, free-space optics, etc.

To improve the input-current-overdrive capability of the TIA and to protect it from saturating, an input-current-signal compression technique, as shown in Fig. 30.9.1, is implemented. The full input-current range is divided into 2 regions: linear and compression. There are 2 important points on this characteristic: the break-point (I_{IN}^B) between linear and compression region of operation and the monotonic maximum (I_{IN}^M) of compression.

When operating in the linear region ($I_{IN} < I_{IN}^B$), the TIA responds linearly to the input current. For the higher input currents ($I_{IN} > I_{IN}^B$), the TIA responds non-linearly and compresses the input current signal.

The basic circuit topology of the TIA with compression is shown in Fig. 30.9.2. The circuit uses fixed shunt-shunt feedback resistor R_f across 2 transistor stages: common-emitter voltage amplifier (Q1) at the input and common-collector voltage buffer (Q2) at the output. When operating in the linear region ($I_{IN} < I_{IN}^B$), the output voltage V_{OUT} is determined by the input current through the fixed feedback resistor R_f: $V_{OUT} \approx R_f(I_{IN} + I_{B1}) + V_{BE1}$. Transistors Q5 and Q4 are off and thus do not affect the linear operation.

When the input current approaches the break-point current I_{IN}^B, transistor Q5 starts to conduct current to the input. This creates a parallel current path with the fixed transimpedance R_f. Thus transistor Q5 dynamically lowers the overall transimpedance of the TIA in response to the input current. This prevents the TIA from saturating. The output voltage V_{OUT}, in the compression region, is determined by the sum of base-emitter voltages of Q5, Q1, and almost-constant voltage drop across R_{C2} and Q2: $V_{OUT} = V_t \ln (I_{IN} I_{C1}/I_S^2) + V_{RC2} - V_{BE2}$, where I_{C1} is the collector current of Q1.

The diode-connected transistors Q3, Q4 create a compensation circuit, which is necessary for small-signal stability over the full input-current range of TIA. In response to the input current, the compensation circuit dynamically lowers the small-signal resistance seen from the collector of Q1. This lowers the open-loop gain of the whole TIA and thus maintains the phase margin of the loop gain. The dynamic compensation works together with the compression and it is inactive in the linear region of operation.

The break point I_{IN}^B between both regions of operation can be adjusted by the ratio of resistors R_{C2}/R_{C1} independently of the fixed transimpedance R_f: $I_{IN}^B \approx (R_{C2}/R_{C1})(V_{CC} - 2V_{BE})/R_f - I_{B1}$, where I_{B1} is the basis current of transistor Q1. I_{IN}^B of the proposed design is ~10µA (see Fig. 30.9.6).

There is also a trade-off between BW and DR in the proposed compression circuit due to the Miller-multiplied capacitance between base and emitter of transistor Q5 (Fig. 30.9.2). However this capacitance is usually very small in modern poly-emitter and poly-base NPN transistors.

The principal schematic of a complete differential-output optical receiver is shown in Fig. 30.9.3. A dummy TIA is used as a voltage reference for the differential amplifier. The large 50pF on-chip capacitor at the output of the reference TIA is used for filtering the noise of the reference. The maximal output differential peak-to-peak voltage is ~1.7V when driving a 50Ω load.

Measured DC-transfer characteristic of the complete circuit is shown in Fig. 30.9.4. The input current is logarithmically swept from 100nA to 20mA with 200 points. Monotonic maximum of compression I_{IN}^M is determined by placing $dV_{OUT}/dI_{IN} = 0$, which results in ~8mA for the proposed design. The frequency response of the complete receiver in the linear region of operation is shown in Fig. 30.9.5. When operating in the linear region, BW is independent of the input current while in the compression region BW increases with input current. This is caused by the transimpedance dependence on the input current. Thus the minimal BW (and maximal transimpedance) of the TIA is in the linear region of operation. This is also clearly seen in Fig. 30.9.6, where the input current pulses have amplitudes linearly swept from 2µA to 20µA with 2µA steps, and logarithmically swept from 40µA to 20mA with 10 points. The full width at half maximum (FWHM) pulse-width of the input current pulses is 5ns with a rise/fall time of 1ns.

The proposed circuit exhibits the highest DR at the input, among other wide-DR TIAs [3-6], while still maintaining a rather high BW.

The complete receiver with 50Ω differential-output driver occupies 1.24mm² in 0.35µm SiGe BiCMOS technology and draws 78mA from a 5V supply. The chip micrograph is shown in Fig. 30.9.7.

The proposed receiver is able to sense the input signal more than 5 orders of magnitude. Moreover, the compression does not affect the noise performance of the TIA and therefore, the low-noise advantage of common-emitter topology can be used to detect a small current at the input.

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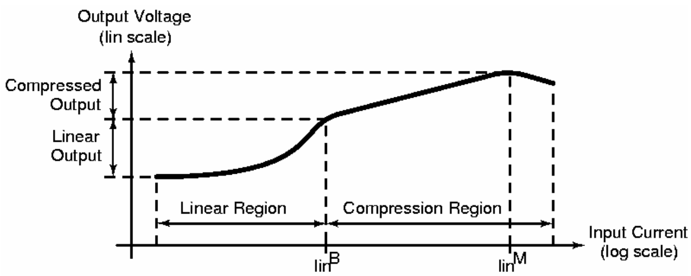

Figure 30.9.1: Regions of operation.

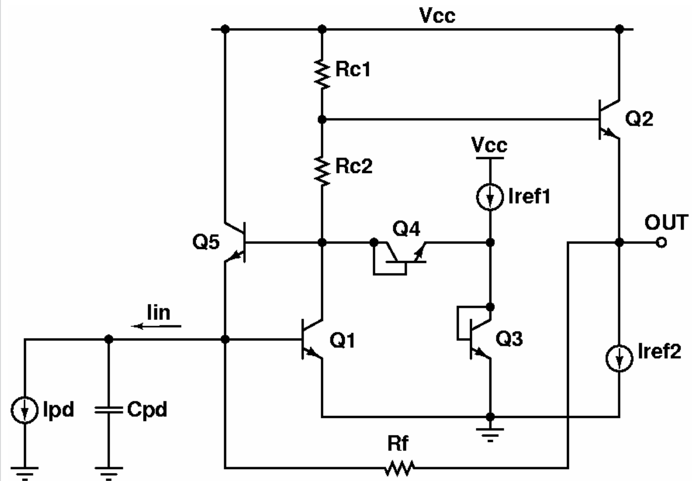

Figure 30.9.2: Basic circuit topology of TIA with compression.

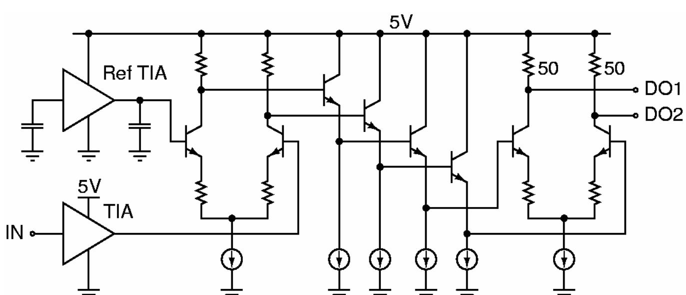

Figure 30.9.3: Circuit diagram of complete optical receiver.

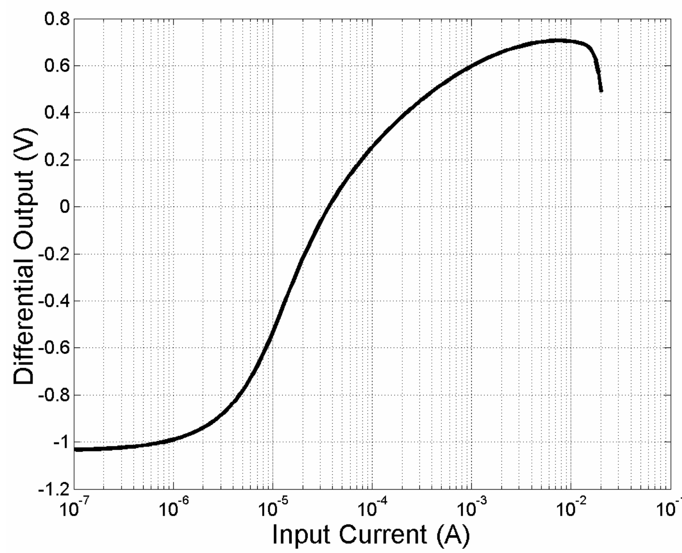

Figure 30.9.4: Measured DC transfer characteristic.

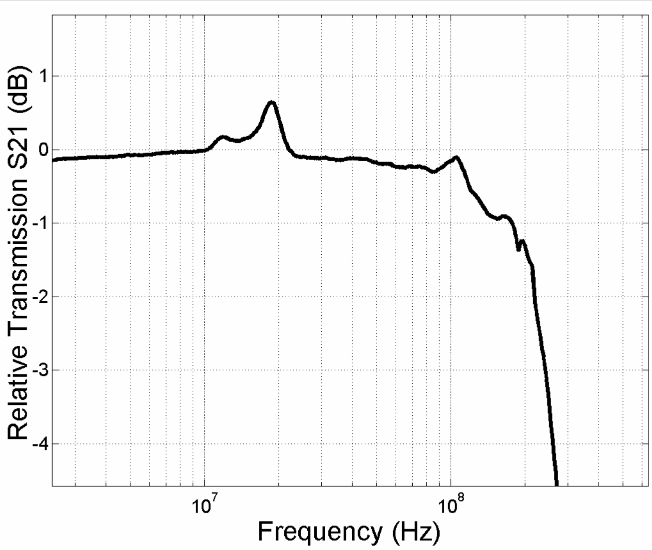

Figure 30.9.5: Measured frequency-response in the linear region of operation.

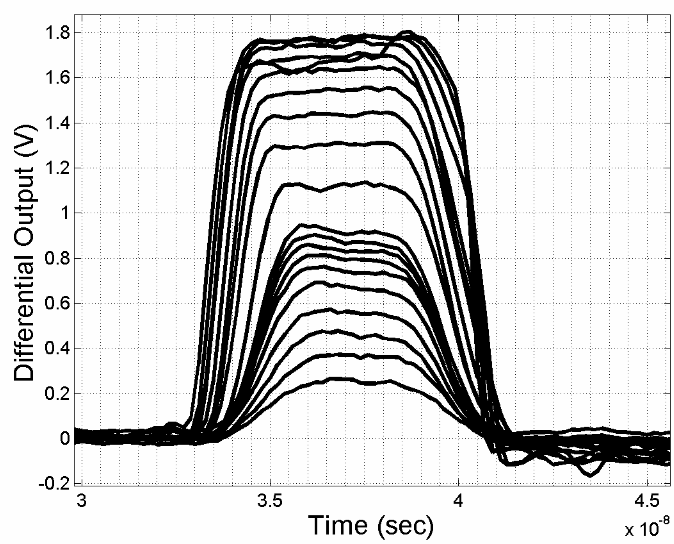

Figure 30.9.6: Measured current pulse responses.

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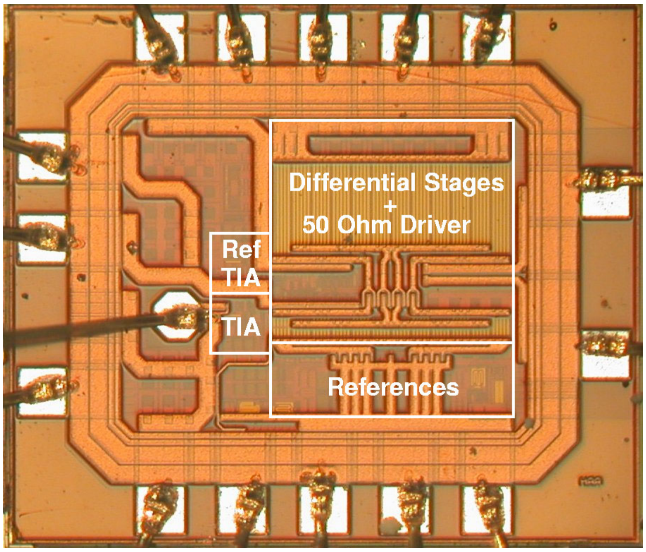

Figure 30.9.7: Micrograph of complete receiver.

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